US-PAT-NO:

5953286

DOCUMENT-IDENTIFIER:

US 5953286 A

TITLE:

Synchronous DRAM having a high data

transfer rate

----- KWIC -----

Detailed Description Text - DETX (13):

The output control clock generating circuit 206 receives the internal clock

ICLK and the discrimination values "0" to "m", and generates a clock FCLK

having the same clock period (namely, frequency) as that of the internal clock

ICLK. Since the internal clock ICLK has the same clock period as that of the

clock CLK, the clock FCLK has the same clock period as that of the clock CLK.

The output control clock generating circuit 206 can adjust the phase of the

output clock OCLK arbitrarily in time. Accordingly, the output control clock

generating circuit 206 can cause the output clock OCLK to have completely the

same clock period and phase as those of the clock CLK, or alternatively to have

a phase in advance to the phase of the clock CLK.

L Number	Hits	Search Text	DB	Time stamp
1	7973		USPAT;	2003/10/22 20:04
			US-PGPUB;	
			EPO; JPO;	
	110714	-N	DERWENT	2002/10/22 20.50
2	119714	phase adj shift\$4	USPAT; US-PGPUB;	2003/10/22 20:50
			EPO; JPO;	
			DERWENT	
3	146	(dll (delay adj lock\$4 adj loop)) near4	USPAT;	2003/10/22 20:08
]		(phase adj shift\$4)	US-PGPUB;	
			EPO; JPO;	
			DERWENT	
4	5406	(phase adj shift\$4) near4 "90"	USPAT;	2003/10/22 20:50
			US-PGPUB; EPO; JPO;	
			DERWENT	
5	13	(dll (delay adj lock\$4 adj loop)) same	USPAT;	2003/10/22 20:58
	13	((phase adj shift\$4) near4 "90")	US-PGPUB;	2000, 10, 22 20.00
		, , , , , , , , , , , , , , , , , , , ,	EPO; JPO;	
			DERWENT	
6	372		USPAT;	2003/10/22 20:58
		(phase adj shift\$4)	US-PGPUB;	
			EPO; JPO;	
7	226	((dll (delay adj lock\$4 adj loop)) same	DERWENT USPAT;	2003/10/22 20:59
'	220	(phase adj shift\$4)) not ((dll (delay adj	US-PGPUB;	2003/10/22 20.39
		lock\$4 adj loop)) near4 (phase adj	EPO; JPO;	
		shift\$4))	DERWENT	
8	3415	transmit adj clock	USPAT;	2003/10/22 20:59
			US-PGPUB;	
			EPO; JPO;	
9	20	/// 411 / 4-1 4- 1	DERWENT	0000/10/00 01 17
9	28	(((dll (delay adj lock\$4 adj loop)) same (phase adj shift\$4)) not ((dll (delay adj	USPAT; US-PGPUB;	2003/10/22 21:17
		lock\$4 adj loop)) near4 (phase adj	EPO; JPO;	
		shift\$4))) and (transmit adj clock)	DERWENT	
10	198		USPAT;	2003/10/22 22:34
		(phase adj shift\$4)) not ((dll (delay adj	US-PGPUB;	
		lock\$4 adj loop)) near4 (phase adj	EPO; JPO;	
		shift\$4))) not ((((dll (delay adj lock\$4 adj loop)) same (phase adj shift\$4)) not	DERWENT	
		((dll (delay adj lock\$4 adj loop)) near4		
		(phase adj shift\$4))) and (transmit adj		
		clock))		
11	812	arbitra\$5 same (phase near2 (adjust\$5	USPAT;	2003/10/22 22:50
		correct\$4))	US-PGPUB;	
			EPO; JPO;	
12	21284	transmit\$4 near3 clock	DERWENT	2003/10/22 22:43
**	21204	Cransmitc4 Hears Clock	USPAT; US-PGPUB;	2003/10/22 22:43
			EPO; JPO;	
			DERWENT	
13	6	(()	USPAT;	2003/10/22 22:43
		correct\$4))) same (transmit\$4 near3	US-PGPUB;	
		clock)	EPO; JPO;	
14	204	nrhitrack noare /whose nearly /	DERWENT	2002/10/22 22-51
14	204	arbitra\$5 near6 (phase near2 (adjust\$5 correct\$4))	USPAT; US-PGPUB;	2003/10/22 22:51
		COLLECTAIL	EPO; JPO;	
			DERWENT	
15	29	(arbitra\$5 near6 (phase near2 (adjust\$5	USPAT;	2003/10/22 22:51
]		correct\$4))) same clock	US-PGPUB;	
			EPO; JPO;	
			DERWENT	